



7/12/96

PCN-962801**

32K×8 SRAM Product Change Notification

Change Description: 0.6μ technology to 0.5μ technology, speed improvement

This letter is to serve as a notification of a product change for Alliance Semiconductor part numbers AS7C256 and AS7C3256. The new 5V and 3.3V 32K×8 product revision is currently in production and applies to all speeds and packages. It is designed to meet or exceed the specifications set forth in the AS7C(3)256 data sheets. The new revision is produced using 0.5μ process technology, a step up from 0.6μ technology used to produce the previous revision.

Highlights of the new 32K×8 SRAM revision:

- Consolidates 5V and 3.3V 32K×8 devices into a single mask set
- Enhanced speed distribution to 10ns (5V) and 12ns (3.3V)
- Mature 8 inch wafer 0.5μ process technology

Alliance has made this revision in order to deliver the most competitive performance and cost effective solution to our customers at the highest levels of quality. Shipments of this revision will commence immediately.

Please contact your local sales representative if you have any questions regarding this information.

Sincerely,

Anwar Khan
Quality Director

Sid Agrawal
Vice President, Marketing

ALLIANCE SEMICONDUCTOR
3099 NORTH FIRST STREET SAN JOSE, CA 95134



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Characterization data for Alliance 32K×8 SRAM revision

Parameter	Description	Vcc	-12		3V -12 data		5V -10 data		-10	units
			spec	25deg	80deg	25deg	80deg	spec		
TAA	address access time	4.4V	12	11	11	8	9	10	ns	
TACE	CE access time	4.4V	12	10	11	8	9	10	ns	
TCW	CE pulse width	4.4V	10	5	5	4	5	9	ns	
TAW	address setup to write high	4.4V	10	6	6	5	6	9	ns	
TAS	address setup to write low	5.6V	0	-2	-2	-2	-2	0	ns	
TWP	write pulse width	4.4V	8	5	5	4	5	7	ns	
TOE	output turn-on time	4.4V	3	2	2	1	1	3	ns	
Icc	Operating current	5.6V	55	19.0	19.0	31.0	31.0	120	mA	
Isb	CMOS standby current	5.6V	20	<0.05	<0.05	<0.05	0.06	45	mA	
Cin	Input capacitance		5	5 max		5 max		5	pF	